NAME

kissis - front end to SIS with an interface to Nelsis

SYNOPSIS

kissis [options] filename

OPTIONS

-h Display help info.

-c Run combinatorial synthesis (PLA or BLIF input formats).

-k Run sequential synthesis (kiss2 input format).

-b Run sequential synthesis (BLIF input format).

-r Run retiming (default not)

-S <filename>

Read the names of special terminals from file (see blif2sls(1SDF) **-c** option).

-x Generate external terminals connected to outputs of all latches. It can be usefull when debugging circuit with *simeye* (see simeye(1ICD)) after layout extraction.

filename

Input filename.

If none of these options is specified then kind of input is determined based on filename extension (default kiss2). If options are specified than extension does not matter. Default extension is .kiss2.

DESCRIPTION

SIS, the Berkeley Logic Synthesis System, is an interactive tool for synthesis and optimization of sequential circuits. Given a state transition table, a logic level description of a sequential circuit or PLA (programmable logic array) decription, it produces an optimized net-list in the target technology while preserving the sequential input-output behavior.

Kissis is a front-end to SIS which allows automatic generation of a circuit for given STG (state transition graph) or PLA. For this purpose it runs SIS in batch mode. Resulting circuit is automatically placed in Nelsis database.

The following design steps are performed:

- State minimization using program called stamina (STG input only).
- State assignment using program called nova (STG input only).
- Combinatorial optimization.
- Technology mapping.
- Retiming (STG input only and when **-r** specified)
- Conversion from BLIF output format to SLS (Switch Level Simulator) using *blif2sls* program, see manual page blif2sls(1SDF).
- Conversion from SLS format to the Nelsis database using *csls* program, see manual page csls(1ICD).

FILES

To run properly the command requires that the following files are present in your current directory:

proto_file

- a file with SLS prototypes (see blif2sls(1SDF)).

<cellname>.<kiss2|pla|blif>

- input file with STG (PLA) description.

Other files:

$OCEAN/celllibs/$OCEANPROCESS/<lib_name>.genlib
- a file with a library description (to be used during technology mapping).

<cell_name>_out.blif
- intermediate file (output in BLIF format).

<cell_name>.sls
- intermediate file (output in SLS format).

<cell_name>.sta
- output from *blif2sls* used by *simeye.*

sis_logfile
- output from *sis* program (look here if something goes wrong).

EXTERNAL_INFLUENCES

Environment Variables:

OCEAN - Root directory of Ocean tree.

OCEANPROCESS
- Ocean process name.

AUTHOR

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SEE ALSO

blif2sls(1SDF), csls(1ICD), simeye(1ICD).

For more information about SIS and its input formats look into:

"SIS: A System for Sequential Circuit Synthesis" Ellen M. Santovich, Kanwar Jit Singh, Luciano Lavagno, Cho Moon, Rajeev Murgai, Alexander Saldanha, Hamid Savoj, Paul R. Stephan, Robert K. Brayton, Alberto Sangiovanni-Vincentelli. Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA 94720. (1992)