NAME

sls - switch-level simulation program

SYNOPSIS

sls [-fmnov] cell commandfile

OPTIONS

The following options can be specified:

-f Force network expansion and generation of new binaries.

-m When the monitoring option is given the program will print run time statistics in a file called "sls.mon".

-n Do not run the network expansion program *sls_exp* before simulation (option **-f** not specified).

-o Only create a new *cell*.out file (no simulation).

-v Print information about actions taken by the program.

DESCRIPTION

Sls is a switch-level simulator, which can simulate the logical and timing behavior of digital MOS circuits. The circuit to be simulated can be described at transistor level, gate level and functional level.

The invocation of *sls* requires two program arguments.

cell This name specifies the network to be simulated.

commandfile This file must contain the input signals for the network and the commands that control the simulation and specify the output format.

In order to simulate a particular cell, a binary format file has to be present for this cell in the database. Default, sls first calls the network expansion program *sls_exp* to generate such a format binary file.

The *sls* program will generate a file called "*cell*.out", which contains the simulation results in readable format. Another output file, "*cell*.res", will contain descriptions of the output signals that can be used as input for a post processor (e.g. *simeye*).

EXAMPLES

```
% sls latch latch.cmd
```

AUTHOR

A.J. van Genderen, A.C. de Graaf

FILES

cell`.out`	output file
cell`.res`	output file
cell`.plt`	(opt.) output file
cell`.dis`	(opt.) output file
`sls.mon`	(opt.) output file

SEE ALSO

A.C. de Graaf, A.J. van Genderen, "SLS: Switch-Level Simulator User's Manual", Delft University of Technology.
O. Hol, "Functional Simulation User's Manual", Delft University of Technology.
cfun(1ICD), csls(1ICD), sls_exp(1ICD), simeye(1ICD).