

Hierarchical Extraction and Terminals

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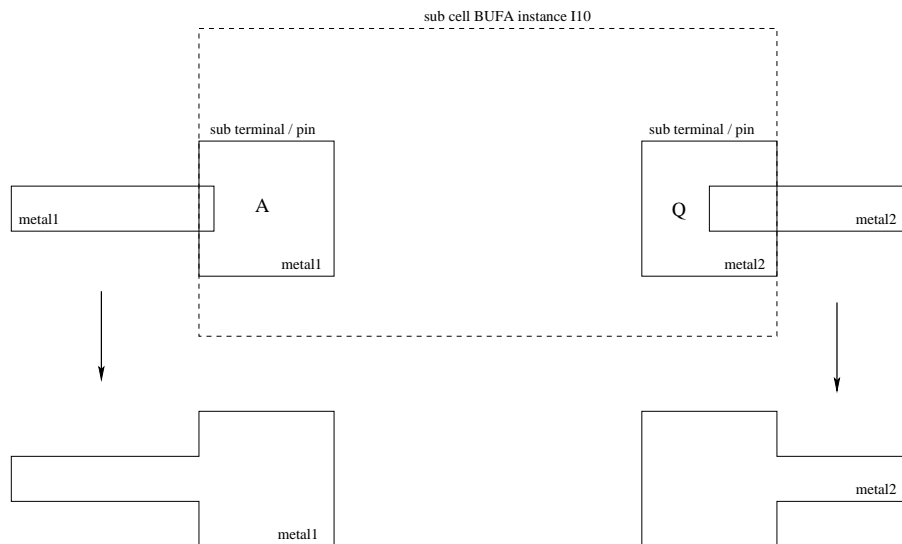
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1. INTRODUCTION

When a hierarchical extraction is performed with the *space* program, then the layout of the sub cells is not taken into account. However, because the layout of the top cell must connect with the terminals of the sub cells (sub terminals or sub cell instance pins). Therefore the layout of the sub terminals is lifted and added to the layout of the top cell. This is done for the mask or layer where in the sub terminals are specified. Therefore the sub terminal mask (conductor) can easily connect with the same mask (conductor) on the top level, when they touch or overlap each other. However, because the sub terminal layout elements are lifted to the top level, the dimension of these terminals is taken into account for parasitics extraction of the top level cell.

See the figure below.



When no sub terminal layout must be added to the top cell layout, the designer has the possibility to use sub terminals which have no dimension. For example, when the sub terminal element has no height and/or width the terminal has no dimension. In that case a connection to the top level layout is only made, when the sub terminal position touches or lays inside the top level mask element.

For example, when sub terminals A and Q have no height and only a width, then a connection is only made when the left x position of sub terminal A is used for its position, but sub terminal Q does not connect. Default, when no resistances are extracted, always the left x and center y position of sub terminals is used. However, when resistances are extracted by the *space* program, then the center x,y position of the sub terminals is used. In that case, in the example above, sub terminal A does not connect, but sub terminal Q does connect. Thus you see, that the used overlap of the layout element of the top level is important. You can use *space* parameter "term_use_center" to choose for another default for the sub terminal positions.

2. USING XCONTROL

When using the *xcontrol* program, the designer can give sub cells a special cell status.

For example the "library" status can be given to sub cells. Even when the layout is flat extracted, these cells are not flattened. For these "library" cells you can specify "free" or "freemasks". These mask elements are added to the extracted layout and thus the library cell pins can easily connect.

For parasitics extraction of only the top level, you must exclude the mask elements of the library cells. Thus, you need to use a boundary box mask for these library cells, to mask out these masks for parasitics extraction. Thus, you can give these elements a zero conductance value in the space technology file. And you can specify that no capacitances must be extracted for these conductance elements.

Note that, when the "macro" status is given to sub cells, then these sub cells are always flattened. This is useful when doing a hierarchical extraction and is normally used for via cells.