NAME

space - 2D hierarchical layout to circuit extractor

SYNOPSIS

space [-cClrzGbFTIuntvhijkx] [-a*time*] [-D*depth*]
[-e*def* | -E*file*] [-p*def* | -P*file*] [-S*param*=*value*] cell

OPTIONS

The following options can be specified:

-c Extract capacitances to substrate (ground).

-C Also extract coupling capacitances, implies **-c**.

-l Also extract lateral coupling capacitances, implies **-C**.

-r Extract resistances for high-resistivity (non-metal) interconnect.

-z Apply mesh refinement for interconnect resistance extraction, implies **-r**.

-G Extract RC models that are accurate up to a certain frequency.

-b Use a simple but fast method to compute substrate resistances.

-F Do *flat* extraction, instead of hierarchical.

-T Only extract the *top* cell (by hierarchical extraction).

-I Unset *incremental* mode: do not skip sub-cells for which the circuit is up-to-date. Cannot be used with the **-F** option.

-D*depth* Selectively unset incremental mode for all cells at level <= *depth* (default *depth* = 1). Cannot be used with the **-F** option.

-u Do not automatically run the preprocessors *makeboxl(1ICD)* and *makegln(1ICD).*

-n Do not apply the circuit reduction heuristics.

-t Add positions of nets, net-names, devices and sub-cells to the extracted circuit.

-v Verbose mode.

-h Print help information.

-i Print statistics, implies verbose mode.

-j Selective resistance extraction, resistances are extracted for all but specified interconnects.

-k Selective resistance extraction, resistances are only extracted for specified interconnects.

-x Generate layout backannotation data, implies **-t**.

-a*time* Make *space* report its progression every *time* seconds.

-e*def* Use the file space.*def*.t in the ICD process library as the element definition file.

-E*file* Use *file* as the element definition file.

-p*def* Use the file space.*def*.p in the ICD process library as the parameter file.

-P*file* Use *file* as the parameter file.

-S*param*=*value*
Set parameter *param* to the value *value*, overrides the setting in the parameter (.p) file. Note that **-S***param* is equivalent to **-S***param*=on.

NOTICE

This manual page only gives a brief introduction to *space*. It should in most cases be sufficient, however, for performing straight-forward extraction tasks. Other documentation is available, see below.

DESCRIPTION

Space is a 2D hierarchical layout to circuit extractor for 45 degree polygonal geometries. The program is capable of accurately extracting MOS and bipolar integrated circuits, including interconnect resistances and capacitances, and substrate resistances. Generally spoken, *space* extracts the circuits for all layout cells that are specified in the cell argument list. These circuits can then be directly simulated, for example, with *sls(1ICD)* or *spice.*

Hierarchical, Flat or Mixed Extraction

The basic extraction mode of *space* is hierarchical. In this mode, the hierarchical structure of the circuit produced is identical to that of the layout. In hierarchical mode, *space* traverses the hierarchy itself. It is thus only necessary to specify the root(s) of the tree(s) to be extracted on the command line. When the **-F** option is used, the layout is flattened before extraction. With hierarchical extraction, only the top cell is extracted and the hierarchy is not traversed when the **-T** option is used. Mixed hierarchical/flat extraction can be accomplished by assigning some cells the *macro* status, see tool *xcontrol(1ICD)* or (old) tool *macro(1ICD).* Cells with the *macro* status are always completely expanded in their parent cells. When all cells would have the macro status, the circuit produced would be the same as when the **-F** option was used.

Incremental Extraction

In hierarchical mode, *space* works incrementally. That is, it only extracts those cells which have not yet been extracted or are out of date with respect to the layout. Incremental mode can be disabled with the **-I** option, in which case *space* extracts all cells in the tree. It can be selectively disabled for all cells at level <= *depth* with the **-D***depth* option. The cells named on the command line are at level 1, their children at level 2, etc. The default *depth* is 1. Thus, the cells named on the command line are extracted even if the circuit exists and is up-to-date with respect to the layout. Use **-D***0* if this is not desirable. The option **-D***infinity* is equivalent to **-I**. The **-I** and **-D***depth* options have no effect in flat extraction mode.

Area/Perimeter based Capacitance Extraction

By default, *space* uses an area/perimeter method for capacitance extraction. The capacitance is assumed to be proportional to c1 ∗ A + c2 ∗ P, where c1 and c2 are constants depending on which masks are present at a certain spot, and A and P are the relevant interconnect areas and perimeters. When using the **-c** option, all capacitances found, including the inter-wire coupling capacitances, are connected to ground (the substrate). When the **-C** option is used, however, the coupling capacitances are put in the extracted circuit.

The formula above only accounts for the coupling capacitances caused by overlapping wires. To also extract the capacitive coupling between neighboring wires, the **-l** option can be used. See the Space User's Manual for details.

Interconnect Resistance Extraction

When extracting interconnect resistances, *space* applies finite element techniques to construct a fine resistance mesh that models resistive effects in detail, and then applies a Gaussian elimination (or, equivalently, a star-triangle transformation) node reduction technique to find the final network. In general, this network contains the nodes that are gate, source or drain connections, and nodes that are connections to instances or terminals of the cell. However, the topology of the network is influenced by the network reduction heuristics that are applied, see below.

When also extracting capacitances, the mesh will be an RC mesh. In this case, the node reduction will proceed such that the Elmore time constants between the nodes in the final network are unchanged with respect to their value in the fine RC mesh. This will guarantee that the electrical transfer function of the final network closely matches that of the fine RC mesh and, consequently, that of the actual circuit.

Network Reduction Heuristics

When extracting resistances and capacitances, *space* can apply some heuristics to further reduce the number of elements (resistors, capacitors and nodes) in the final network by neglecting irrelevant detail. These heuristics include

1. Merging of nodes that are connected by small resistance.
2. Deletion of large shunt resistances.

3. Reconnecting small coupling capacitances to ground.

All heuristics are controlled by parameters from the parameter file (see below).

Selective Resistance Extraction
Selective resistance extraction is possible by specifying some interconnects in a file called 'sel_con' and by using either the option **-k** or **-j.** When using the option **-k,** resistances will only be extracted for the interconnects that are specified in the file 'sel_con'. When using the option **-j,** resistances will be extracted for all interconnects except for the interconnects that are specified in the file 'sel_con'. The format of the latter file is as follows. On each line, an x position, an y position and a maskname is specified. When an interconnect has the specified mask on the specified layout position, that interconnect is specified in the file. As an alternative also a netname can be specified on each line, the netname must have a leading '=' character. The netname may begin or end with a '*' wildcard character.

Library Cell Circuit Extraction
When a layout description contains cells that need not to be extracted because a separate circuit or behavioral description is available for them (e.g. standard cells, gate arrays) these cells should be set to the *library* or *device* status. For new projects, the status is set by using tool *xcontrol(1ICD).* Note that for old projects the device status was set by tool *device(1ICD).* For the library cells a circuit view must already exist. For device cells, use tool *putdevmod(1ICD)* to put device descriptions in the circuit view. When the device/library status is defined for a layout cell, *space* will not extract this cell but it will include it as a network primitive in the extracted circuit. This will work both with hierarchical and flat extractions.

Simulation Model Support
Simulation models can be specified for the devices that are extracted by using the control file of *xspice(1ICD).*

Element Definition File
Space is technology independent. At start up, it reads a tabular element definition file specifying how the different elements like conductors and transistors can be recognized from the different mask combinations, and which values should be used for for example conductor capacitivity and conductor resistivity. This tabular element file is constructed from an user-defined element definition file by the *space* technology compiler *tecc*(1ICD).

The default element definition file is *space.def.t* in the appropriate directory of the ICD process library. However, there can be several other element definition files for a particular process. For example, the file *space.max.t* may contain an element description with worst-case capacitance and resistance values. This file can be read rather than the standard file by specifying **-e***max* at the command line.

You can also prepare your own element definition file and specify the name of that file with the **-E***file* option. For a description of the format of such a file, see the Space User's Manual.

Parameter File
Much of the operation of *space* is also under control of parameters that are specified in a parameter file. The default parameter file is *space.def.p* in the appropriate directory of the ICD process library. You can select another parameter file with the **-p***def* or the **-P***file* options, analogous to selecting another element definition file.

Information Feedback
The **-v** option produces information on what files *space* is reading and what extraction steps are being taken. The **-i** option produces quantitative information, such as the number of nets and transistors. With the **-a***time* option, *space* reports its progression, in percentage of the layout scanned, every *time* seconds. *Space* also reports its progression when it receives an ALARM signal, such a signal can be send by the command "kill -ALRM *pid*", where *pid* is the process id.

Implementation
Space is a scanline based extractor. As a scanline is swept over the layout plane, the different steps of the method are executed in one pass. While the RC mesh is being constructed from the layout, nodes are eliminated as soon as all resistances and capacitances for that node are known. Also, all network elements are

written to the database as soon as possible. This results in low time and space complexities of O(N) and O(sqrt(N)) respectively, where N is the number of contour edges of the interconnection polygons.

Different Versions of Space
Use the *space3d(1ICD)* version for 3D capacitance extraction using a boundary-element method and for accurate substrate resistance extraction using a boundary-element method.

Space System User Interface
The program *helios(1ICD)* can also been used. It is an User Interface for tool execution, build around the Space System. You don't need to remember the options needed to run an extraction. You can easy use the Extract Option Forms and click with the mouse on the buttons. You can also edit a layout cell using tool *dali(1ICD)* with it. You can also make a netlisting or run a circuit simulation using tool *simeye(1ICD)* with it.

EXAMPLES

Produce a transistor network for the cell *latch*:

% space latch

Include substrate (ground) capacitances:

% space -c latch

Also include coupling capacitances and resistances:

% space -Cr latch

SPECIAL CONSIDERATIONS

Before performing the actual extraction, *space* first runs the preprocessors *makeboxl(1ICD)* and *makegln(1ICD)* to convert the original layout information into a set of non-vertical line segment files (gln files). When needed, also the *makesize(1ICD)* preprocessor is called for resizes and new gln masks. This is automatically done by the *space* program.

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FILES

`ICDPATH/share/lib/process/`*process*`/space.def.t`
: default element definition file

`ICDPATH/share/lib/process/`*process*`/space.def.p`
: default parameter file

`NELSISPROJECT/exp_dat`
: list of cells to be extracted

SPACE_TMPDIR

Space uses a directory where it stores temporary data. The default directory for this is selected from the list of directories "/tmp" and "/usr/tmp", whichever has more space available. Using the environment variable `SPACE_TMPDIR` it is possible to specify an alternative list of directories, separated by the character ':' or ';'. For example:

% setenv SPACE_TMPDIR /tmp:/usr/tmp:/user/john/tmp

SEE ALSO

N.P. van der Meijs, A.J. van Genderen, F. Beeftink and P.J.H. Elias, "Space User's Manual", Delft University of Technology, Delft, The Netherlands.

N.P. van der Meijs and A.J. van Genderen, "Space Tutorial", Delft University of Technology, Delft, The Netherlands.

S. de Graaf, N.P. van der Meijs and A.J. van Genderen, "Space Tutorial Helios Version", Delft University of Technology, Delft, The Netherlands.

A.J. van Genderen, N.P. van der Meijs and T. Smedes, "Space Substrate Resistance Extraction User's Manual", Delft University of Technology, Delft, The Netherlands.

helios(1ICD), makeboxl(1ICD), makedela(1ICD), makegln(1ICD), makemesh(1ICD), makesize(1ICD), putdevmod(1ICD), space(4ICD), space3d(1ICD), tecc(1ICD), xcontrol(1ICD).