NAME
>   blif2sls - convert a BLIF file to SLS format

SYNOPSIS
>   **blif2sls** [options] [network_name]

OPTIONS

>   **-h**   Display help info.

>   **-v**   Verbose mode for parser.

>   **-a**   Create <network>.sta file (see simeye(1ICD)).

>   **-x**   Generate external terminals connected to outputs of all latches. It can be usefull when debugging
>   circuit with *simeye* (see simeye(1ICD)) after layout extraction.

>   **-b <filename>**
>   Take input from file.

>   **-s <filename>**
>   Send output to file.

>   **-i <filename>**
>   Alternative prototype file (default: oplib1_93.ext).

>   **-c <filename>**
>   Read the names of special terminals from file.

>   **network_name**
>   Name of the network to be converted. It searches for input file called <network_name>.blif and
>   writes output to <network_name>.sls. No other options are required.

>   If only one of **-b** and **-s** options is used then stdin (or stdout) is used instead.

DESCRIPTION

>   SIS, the Berkeley Logic Synthesis System, is an interactive tool for synthesis and optimization of sequential
>   circuits. Given a state transition table, a logic level description of a sequential circuit or PLA description, it
>   produces an optimized net-list in the target technology while preserving the sequential input-output behavior.

>   This program converts an output from SIS in BLIF (Berkeley Logic Interchange Format) format to SLS
>   (Switch-Level Simulator) format. The following information from BLIF is used:

>   -   model name

>   -   names of output and input terminals.

>   -   gates, latches and interconnections between them.

>   -   latch order and state coding - only if latches are present and retiming in SIS didn't change initial STG
>   (State Transition Graph). Information about it is printed to file <network>.sta and can be used in *simeye*
>   (see simeye(1ICD)).

>   To determine the right terminals order in the network to be generated, *blif2sls* uses a prototype file which
>   should be present in the current directory. It should contain prototypes of all the networks which are
>   present in the library and could be used by SIS. If some of gates' terminals are not used, they will be left
>   unconnected. For example Q–inverted output from a flip–flop - if not used it could look like this:

>   prototype:

>   extern network dfr11 (terminal D, R, CK, Q, QN, vss, vdd)

and its call:

{inst0} dfr11 (n_2370_, R, CK, LatchOut_v3, , vss, vdd);

Some of the terminals in networks do not have any logical function (e.i. power, clock, reset) - this is at least the case during sequential synthesis. Therefore they are not considered in SIS and do not appear in BLIF file. Still however to obtain a working circuit we need to connect these terminals with the rest of the world. Therefore if any of our cells uses them, they will appear in the list of terminals of just created circuit. These terminals are recognized by looking at the names in the prototypes. The key names are: vdd, vss, R, CK. If you would like to extend this list or define a new one, you can use **-c** option followed by a filename. Inside this file you should place the list of names, separated with white space.

It is important that the prototypes have the same names of terminals as these ones that are defined in genlib library specification used in SIS.

FILES

        <network_name>.blif   - input BLIF file.

        <network_name>.sls   - output SLS file.

        <network_name>.sta   - latch order file.

        <prototypes>.ext   - file with SLS network prototypes.

AUTHOR

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SEE ALSO

        kissis(1SDF), csls(1ICD), simeye(1ICD).

For more information about SIS and its interchange formats look into:

"SIS: A System for Sequential Circuit Synthesis" Ellen M. Santovich, Kanwar Jit Singh, Luciano Lavagno, Cho Moon, Rajeev Murgai, Alexander Saldanha, Hamid Savoj, Paul R. Stephan, Robert K. Brayton, Alberto Sangiovanni-Vincentelli. Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA 94720. (1992)