

NAME

slsmod - process file for *sls*

DESCRIPTION

The file *slsmod* contains the process information for the *sls* simulator. This file is used by *sls* when a simulation is done at level 2 or level 3.

The following variables are used in an *slsmod* process file:

<i>vh</i>	The positive supply voltage in the circuit ($v_l = 0$ is assumed).
<i>vswitch</i>	Switching voltage for O to I and I to O transitions. If this variable is not specified, $vswitch = vh/2$ is used.
<i>vminh</i>	Minimum stable voltage for a logic I state.
<i>vmaxl</i>	Maximum stable voltage for a logic O state.
<i>krise</i>	Factor with which RC time constants for rising voltages are multiplied during timing simulation.
<i>kfall</i>	Factor with which RC time constants for falling voltages are multiplied during timing simulation.
<i>loffset</i>	Value which has to be subtracted from the layout-specified length of a transistor to gain the effective length of the transistor.
<i>woffset</i>	Value which has to be subtracted from the layout-specified width of a transistor to gain the effective width of the transistor.
<i>rstat</i>	The resistance between drain and source used for stable voltage determination.
<i>rsatu</i>	The same resistance but now for the saturated case. A transistor is said to be saturated when - after an initial calculation with <i>rstat</i> resistances - it appears that V_{drain} or $V_{source} > vswitch$ (for <i>nenh</i> transistors) or V_{drain} or $V_{source} < vswitch$ (for <i>penh</i> transistors).
<i>cgstat</i>	The gate capacitance of the transistor used for stable voltage determination.
<i>cgrise</i>	The gate capacitance of the transistor used for rise time calculations.
<i>cgfall</i>	The gate capacitance of the transistor used for fall time calculations.
<i>cestat</i>	The drain or source capacitance of the transistor used for stable voltage determination.
<i>cerise</i>	The drain or source capacitance of the transistor used for rise time calculations.
<i>cefall</i>	The drain or source capacitance of the transistor used for fall time calculations.
<i>rdyn</i>	The resistance between source and drain used for rise and fall time calculations.
<i>cch</i>	The drain or source capacitance of the transistor which is used in addition to <i>cerise</i> or <i>cefall</i> during rise and fall time calculations. However, this capacitance is only used if the transistor is conducting.

First the general simulation parameters *vh*, (eventually *vswitch*), *vminh*, *vmaxl*, *krise* and *kfall* are specified in the *slsmod* file. Next, the other parameters - which are the transistor model parameters - are specified.

Transistor model parameters can be specified for a *nenh*, a *penh* and a *ndep* transistor. Each of these parameter specifications might be omitted but their order is fixed.

For each transistor first a specification of *loffset* and *woffset* is done. Then the other variables are specified by giving their value for some typical transistor dimensions. This is done by first specifying the values for a minimum width and length and then specifying the values for a width and length that only differ from the first width and length by that the width is larger or that the length is larger.

In order to obtain the parameters for transistors that have dimensions that are not enumerated, *sls* will perform an interpolation.

For each transistor there is one general parameter specification list and several mode parameter specification lists. The general specification list contains the values for *rstat*, *cgstat*, *cgrise*, *cgfall*, *cestat*, *cerise* and *cefall*, and the mode specification lists contain the values for *rdyn* and *cch*.

For the nenh transistor and the penh transistor *rdyn* and *cch* have to be specified for the following modes:

<i>pullup</i>	A transistor is in the pullup mode when there is static current flow through it and when a time constant for a falling voltage is determined.
<i>pulldown</i>	A transistor is in the pulldown mode when there is static current flow through it and when a time constant for a falling voltage is determined.
<i>passup</i>	A transistor is in the passup mode when there is no static current flow through it and when a time constant for a rising voltage is determined.
<i>passdown</i>	A transistor is in the passdown mode when there is no static current flow through it and when a time constant for a falling voltage is determined.

Whether or not there is a static current flow through a transistor is determined by considering all transistors to be "on".

For an ndep transistor *rdyn* and *cch* have to be specified for the modes:

<i>load</i>	A transistor is in the load mode when its gate is connected to its drain or source (via a resistor).
<i>superload</i>	A transistor is in the superload mode when its gate is not connected to its drain or source (via a resistor).

EXAMPLE

Below an example of a slsmod file for a NMOS process is given.

```

/* process : nmos4u700A TU-Delft
/* author : A.J. Schooneveld, TU-Delft
/* date : 6 May 1987
*/

vh=5
vminh=4
vmaxl=1
krise=0.90
kfall=0.66

nenh
  loffset=0.625u
  woffset=0.88u
  w=6u l=4u : rstat=4.97k rsatu=25.4k
    cgstat=13.0f cgrise=9.2f
    cgfall=12.0f cestat=2.2f
    cerise=2.4f cefall=2.9f
  w=15u l=4u : rstat=1.69k rsatu=6.95k
    cgstat=48.8f cgrise=24.2f
    cgfall=38.0f cestat=6.3f
    cerise=5.6f cefall=8.9f
  w=30u l=4u : rstat=0.832k rsatu=3.19k
    cgstat=92.1f cgrise=54.1f
    cgfall=82.2f cestat=12.8f
    cerise=11.8f cefall=15.0f
pullup
  /* not determined */

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    w=6u l=4u : rdyn=22.3k cch=8.7f
    w=15u l=4u : rdyn=5.3k cch=31.8f
    w=30u l=4u : rdyn=2.2k cch=53.3f
end
pulldown
    w=6u l=4u : rdyn=22.3k cch=8.7f
    w=15u l=4u : rdyn=5.3k cch=31.8f
    w=30u l=4u : rdyn=2.2k cch=53.3f
end
passup
    w=8u l=4u : rdyn=7.94k cch=4.62f
end
passdown
    w=8u l=4u : rdyn=5.24k cch=5.29f
end
end

ndep
loffset=0.605u
woffset=1.2u
w=6u l=4u : rstat=29.2k rsatu=29.2k
    cgstat=7.8f cgrise=10.7f
    cgfall=23.4f cestat=0f
    cerise=0f cefall=0f
w=6u l=10u : rstat=76.5k rsatu=76.5k
    cgstat=11.7f cgrise=19.8f
    cgfall=28.2f cestat=0f
    cerise=0f cefall=0f
w=12u l=4u : rstat=10.2k rsatu=10.2k
    cgstat=16.4f cgrise=31.7f
    cgfall=46.0f cestat=0f
    cerise=0f cefall=0f
load
    w=6u l=4u : rdyn=25.5k cch=-3.6f
    w=6u l=10u : rdyn=66.3k cch=-14.9f
    w=12u l=4u : rdyn=8.7k cch=-15.9f
end
superload
    w=12u l=4u : rdyn=3.63k cch=-15.6f
end
end

```

AUTHOR

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SEE ALSO

A.J. Schooneveld, "Determination of SLS transistor model parameters", Delft University of Technology, sls(1ICD).