NAME

dimcheck - do a complete design_rule check

SYNOPSIS

dimcheck [-v] [**-c**|**-n**] [**-f**] [**-t**] [**-g**] [cell_name]

OPTIONS

-v verbose mode

-c Perform hierarchy_checks on the cell: i.e. check if connections between sub_cells are made via terminals and check if no elements are formed from primitives from different sub_cells. (default).

-n Do not perform hierarchy_checks.

-t Debugging option, do not filter or merge error messages for a non orthogonal layout.

-g Report gap errors between elements of the same group.

-f Use files 'booldata', 'dimcheckdata1', 'dimcheckdata2' and 'dubcheckdata' if present in the current working directory instead of the standard ones from the library.

DESCRIPTION

Dimcheck checks the layers of a cell definition for all design rule errors. Width, gap and overlap checks are performed and eventually an hierarchy_check. Gap errors between edges of the same group are usually suppressed; use the -g option if this is not desired.

The program *dimcheck* can be used after *exp*.

Checking is carried out in three steps performed by three subprograms, which are called automatically. First the subprogram *nbool* is called to produce the "bool_BN" files and to perform an hierarchy_check. The latter is only significant if the cell to check has been expanded hierarchically. After that the subprograms *dimcheck* and *dubcheck* are called which use these files, together with the "LC_vln" files to do the actual checking for width, gap and overlap errors. The errors are reported on standard output.

If no cell_name is specified the names of the cells to be checked will be read from the file "exp_dat".

The current working directory must be the project directory.

AUTHOR

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FILES

`ICDPATH/share/bin/nbool`
executable

`ICDPATH/share/bin/dimcheck`
executable

`ICDPATH/share/bin/dubcheck`
executable

`ICDPATH/share/lib/process/TECHN/booldata`
(TECHN=technology directory)

`ICDPATH/share/lib/process/TECHN/dimcheckdata2`

`ICDPATH/share/lib/process/TECHN/dubcheckdata`

`NELSISPROJECT/exp_dat`
names of cells to be checked

`NELSISPROJECT/layout/cell/LC_vln`
input files, LC=LayerCode

`NELSISPROJECT/layout/cell/bool_BN`
input files, BN=BooleanNr

SEE ALSO

T.G.R. van Leuken, J. Liedorp "An Hierarchical and Technology Independent Design Rule Checker", Delft University of Technology,
autocheck(1ICD), booldata(4ICD), dimdata(4ICD), dubdata(4ICD), exp(1ICD), nbool(1ICD)

BUGS

It is understood that the design rules are consistent. Error reporting is rather poor; the kind of error (width, gap or overlap) is reported together with the coordinates of the two points between which the error occurred. In case of non orthogonal layouts the errors reported may be shifted a little from the place where they occurred due to rounding errors.