NAME

space3d - 3D hierarchical layout to circuit extractor

SYNOPSIS

space3d [all space options] [-3BUX] [-s scenefile] cell

OPTIONS

The following additional options can be specified:

-3 Use a boundary-element technique for 3-dimensional capacitance extraction. Use with **-c** or **-C** option.

-B Use a boundary-element technique to compute substrate resistances.

-U No calculation of Green's functions and no Schur matrix inversion.

-X Start tool *Xspace*(1ICD) to display the used mesh, etc.

-s *scenefile*

Output a *scene* description of the extraction process. This description contains drawing primitives which can be viewed using the tool *view3d*(1ICD). If the file name has no extension, then ".scn" is added.

NOTICE

This manual page only gives a brief introduction to *space3d*. It should in most cases be sufficient, however, for performing straight-forward extraction tasks. Other documentation is available, see below.

DESCRIPTION

Space3d is a 3D hierarchical layout to circuit extractor for 45 degree polygonal geometries. The program is capable of accurately extracting MOS and bipolar integrated circuits, including interconnect resistances and capacitances, and substrate resistances. Generally spoken, *space3d* extracts the circuits for all layout cells that are specified in the cell argument list. These circuits can then be directly simulated, for example, with *sls(1ICD)* or *spice.*

Space3d is an upgraded version of the fast *space* extractor. For all common behaviour see the manual page of *space(1ICD)* and the Space User's Manual for details.

Three-Dimensional Capacitance Extraction

Space3d can perform very accurate capacitance extraction by using a three-dimensional boundary element method. This is a numerical technique capable of numerically solving the Laplace equation which governs the electrical field around the interconnections wires on the IC. This capability is fully explained in a separate document, and is not discussed here any further.

Three-Dimensional Substrate Extraction

Space3d can perform very accurate substrate resistance and capacitance extraction by using a three-dimensional boundary element method. In modern analog circuits and mixed digital/analog circuits, coupling effects via the substrate can be an important cause of malfunctioning of the circuit. Therefor, the extraction of an accurate substrate model is very important.

Element Definition File

For 3D capacitance extraction the following special sections must be added to the technology file:

vdimensions

The vertical dimension list specifies for different conductors under different mask conditions (1) the distance between the ground plane (substrate) and the bottom of a mask conductor and (2) the thickness of that conductor.

dielectrics

The dielectric structure of the chip. The first dielectric layer starts at the bottom (ground plane)

and all other layers start at a positive vertical position. Each layer has a relative permittivity value.

eshapes Optional, an edge shape list may be specified (see 3D Capacitance User's Manual).

cshapes Optional, a cross-over shape list may be specified (see 3D Capacitance User's Manual).

For 3D substrate resistance extraction the following special section must be added to the technology file:

sublayers
Specifies the conductivity of the substrate (see Substrate Resistance User's Manual).

For 3D substrate capacitance extraction the following special section must be added to the technology file:

subcaplayers
Specifies the relative permittivity of the substrate (see Substrate Resistance User's Manual).

Parameter File

Much of the operation of *space3d* is also under control of parameters that are specified in a parameter file.

The special 3D capacitance parameters start with a leading "**cap3d.**" (see 3D Capacitance User's Manual).

The special 3D substrate resistance parameters start with a leading "**sub3d.**" (see Substrate Resistance User's Manual).

EXAMPLES

To produce a transistor network for the cell *latch* including non-metal resistances and accurate substrate resistances and 2D couple capacitances, type:

% space3d -rBC latch

To produce a transistor network for the cell *latch* including non-metal resistances and with 3D couple capacitances, type:

% space3d -rC3 latch

SPECIAL CONSIDERATIONS

Before performing the actual extraction, beside the preprocessors, for accurate substrate extraction *space3d* first runs a prepass and after that the *makesubres(1ICD)* and if requested the *makesubcap(1ICD)* program.

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FILES

`ICDPATH/share/lib/process/`*process*`/space.def.t`
default element definition file

`ICDPATH/share/lib/process/`*process*`/space.def.p`
default parameter file

`NELSISPROJECT/exp_dat`
list of cells to be extracted

`SPACE_TMPDIR/space[12].xxxxxx`
green buffer temporary files

SEE ALSO

N.P. van der Meijs, A.J. van Genderen, F. Beeftink and P.J.H. Elias, "Space User's Manual", Delft University of Technology, Delft, The Netherlands.

N.P. van der Meijs and A.J. van Genderen, "Space Tutorial", Delft University of Technology, Delft, The Netherlands.

S. de Graaf, N.P. van der Meijs and A.J. van Genderen, "Space Tutorial Helios Version", Delft University of Technology, Delft, The Netherlands.

A.J. van Genderen and N.P. van der Meijs, "Space 3D Capacitance Extraction User's Manual", Delft University of Technology, Delft, The Netherlands.

A.J. van Genderen, N.P. van der Meijs and T. Smedes, "Space Substrate Resistance Extraction User's Manual", Delft University of Technology, Delft, The Netherlands.

helios(1ICD), makesubcap(1ICD), makesubres(1ICD), space(1ICD), tecc(1ICD), view3d(1ICD), Xspace(1ICD).